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Low Power, Noise-Free 4/5 PrescalarUsing Domino Logic

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ABSTRACT: Reduction of propagation delay is very important for high speed applications. This paper gives an idea about the delay reduction on divided-by-4/5 counter. The delay is reduced by domino logic. Dynamic domino logic circuits are widely used in advanced digital Very Large Scale Integration (VLSI) circuits because it is uncomplicated to implement and low cost. Domino logic is a CMOS based approximation of the dynamic logic techniques. It was technologically advanced to speed up the circuit. Compare to static Complementary Metal Oxide Semiconductor (CMOS) logic, dynamic domino logic deals better performance. Domino gates naturally consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static Complementary Metal Oxide Semiconductor (CMOS) gate. In this paper, dynamic logic flip-flop such as Extended True-Single-Phase-Clock (E-TSPC) flip-flop based divided-by-N/N+1 counter is used for high speed and low power applications. And the proposed work is then compared with the static Complementary Metal Oxide Semiconductor (CMOS) logic.

Keywords: D-Flip Flop, Extended True Single Phase clock, Low power, High speed.

I. INTRODUCTION

In VLSI technology miniaturization in size of the circuit has incremented dramatically. This has made it technologically achievable for high speed applications. To achieve this, a high speed frequency divider is required which operate at high input frequency. In modern wireless communication systems, the power consumption is a key factor consideration which increases longer battery life. Generally MOS current mode logic (MCML) circuit, are used for high frequency operation which consumes high power, while a true single phase clock (TSPC) dynamic circuit, consumes only little power during switching in static condition power is minimum, has a minimum operating frequency. [13].

For high frequency operation Elongated True Single Phase Clock (E-TSPC) is used. A prescaler is the most injuctively authorizing part in this high speed frequency divider as it consumes high potency. Dual modulus prescaler consists of flip-flop predicated divided-by-N/N+1 counter. It is acclimate to Elongated-True Single Phase Clock (E-TSPC) Flip-Flops for high speed and low power applications.

By cumulating two different techniques, there is a possibility of getting higher speed of the circuit. This can be done by interconnecting the elongated true single phase clock of dual modulus prescaler with some extra logic. Due to the incorporation of adscititious logic gates between the flip-flops to achieve the two division ratios, the speed of the prescaler is affected and the switching power increases [7].

II. TSPC AND E-TSPC PRESCALERS

Maximum operating frequency with low power dissipation of the TSPC and the E-TSPC predicated flip flop is analyzed .True Single Phase Clock has the advantages of simple and compact clock distribution, high speed and logic design flexibility [1].

There is no clock skew quandary as in C^2MOS because it utilizes single clock phase. But the main disadvantages of this true single phase clock is number of transistor used increases which increases propagation delay.

To overcome from this Elongated True Single Phase Clock is used for low power and high frequency applications which abstracts transistor stacked structure so that all the transistors are free of body effect.

Main advantages of this E- TSPC is it utilizes two transistors. So it has higher operating frequency compared to true single phase clock. The propagation delay of the Elongated True Single Phase Clock (E-TSPC) techniques is more minuscule than the True Single Phase Clock (TSPC) techniques [13]. The Elongated True Single Phase Clock uses two transistors while a True Single Phase Clock uses three transistors as shown in fig 1.

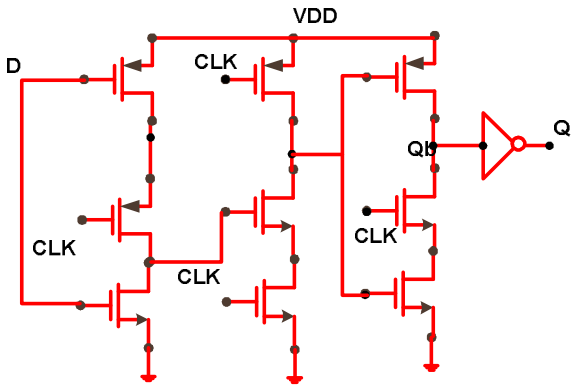

Fig. 1. TSPC D-Flip flop.

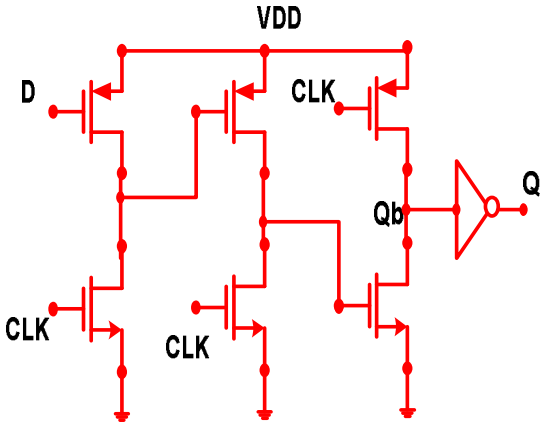

Fig. 2. E-TSPC D-Flip flop.

III. PRESCALER IN DUAL MODE

When amalgamating two different counters in the form of N/N+1 prescalar a dual modulus counter will engendered. This dual modulus prescaler is designed by utilizing high speed low power D-Flip-flop (DFF). The counter is adscititiously called as prescalar which it is utilized for the high frequency electronic circuit. A counter is nothing more than a specialised register or pattern engenderer that engenders a designated output pattern or sequence of binary values upon the application of an input pulse signal called the "Clock". The clock is genuinely utilized for data transfer in these applications. Counters are composed by connecting flip-flops in cascade and any number of flip-flops can be connected or "cascaded" together to compose a "divide-by-n" binary counter where "n" is the number of counter stages used and which is called as Modulus of counter

IV. BLOCK DIAGRAM DIVIDE-BY-4/5 PRESCALAR

The divide-by-4/5 prescaler is the synchronous sequential circuit. The sequential logic circuits are used as data storage purpose. The D-flip-flop is widely used for many electronic devices. It is also known as data (or) delay flip-flop. So, the divide-by 4/5 prescaler is constructed with D-Flip-Flop.

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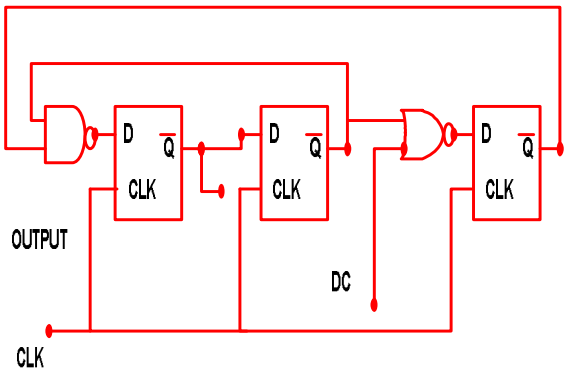

Fig. 3. Divided -by-4/5 prescalar.

The circuit shown in Fig. 3 is the divide-by-4/5 counter using D flip-flop. It consists of three series added flip-flops. The first two flip flops are used as divide-by-4 counter. The third flip-flop with switch control is used as divide-by-5 counter. The NAND gate is utilized to connect the divide-by-4 as the input and the switched control NOR gate is used to connect the output of divide-by-4 counter to the input of divide-by-5 counters [16]. Here when the clock goes to high the output of the divide-by-4/5 counter is high. When the clock signal is goes to low the output of the counter goes to high and low respectively. This divide-by-4/5 counter is proposed in the Elongated True Single Phase Clock form. Due to the radioed method, this D flip-flop circuit only utilizes six MOS transistors in three stages. Because of the series of MOS transistors from the voltage supply to ground is reduced, it can operate at a high frequency. When applying supply voltage the circuit becomes to operate at high speed. Then this circuit is implemented with domino logic for low power applications.

V. DOMINO LOGIC / C^2MOS LOGIC

Domino logic uses fast N- transistor to increase the speed of the circuit. Where the static logic uses slow P-transistors to compute logic. To increase the speed and area efficiency domino gates are often employed in high performance circuits. Due to its performance and CMOS power consumption domino logic has created a considerable interest.

Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [16]. But they have races problem and clock overlapping problem. to overcome this C^2MOS logic is adopted it removes the race problem but still clock overlapping is creating a problem then rearrangement of C^2MOS logic is done in a manner that only two transistor are present in stage this is called as TSPC.

VI. CONCEPT OF C^2MOS LOGIC

Domino logic requires two phases to operate any logic first precharge phase and second evaluation phase. When clock is low output is high, the precharge phase will occur and when the clock is high the evaluation phase will occur. Domino logic is a CMOS based evaluation of the dynamic logic techniques which are based on the either PMOS or NMOS transistors. It was developed to speed up the circuits [17]. The dynamic gate outputs connect to one inverter, in domino logic. In domino logic, cascade structure consisting of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clk cycle), just as dominos, once fallen, cannot stand up. The structure is hence called domino CMOS logic as in figure 4.[18].

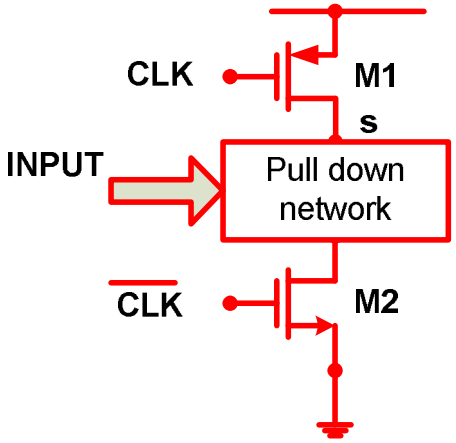

Fig. 4. Domino Logic.

In the Precharge phase when the clock CK is low, the dynamic node S is charged to logic high through M1 and the output of the gate Q is low. The evaluation phase starts when the clock goes high. In this phase, M1 is OFF and M2 is ON.

The dynamic node S discharges or retains its charge depending on the inputs to the pull-down network. Since there are cascaded logic blocks, the evaluation of a stage causes the next stage to evaluate arid so on [19]. All of the above the disadvantage associated with Domino logic is the Race condition and the clock overlapping. Race arise due to continuous connection in between input and output during recharge phase and evaluation phase. C^2MOS logic whose block diagram is shown in figure 5.

A D-Flip-flop design using C^2MOS logic is shown in figure 6. And the conditional structure which arise during Precharge and evaluation phase to remove race is shown in figure 8. In this figure either Pull network or Pull down network connected to output.

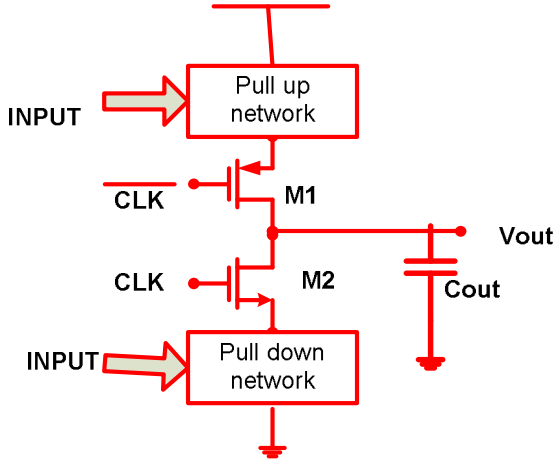

Fig. 5. C^2MOS logic.

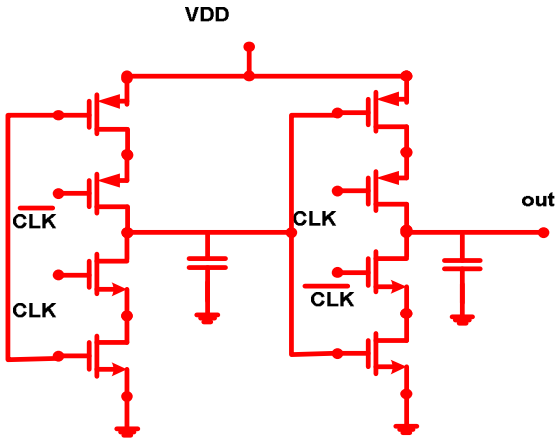

Fig. 6. C^2MOS logic D-Flip flop.

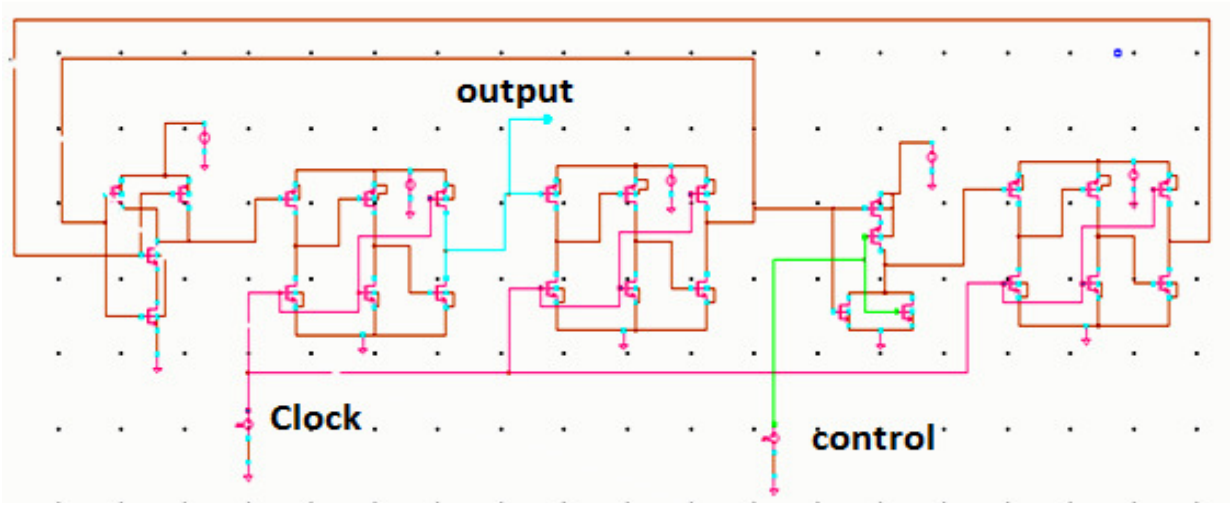

Fig. 7. 4/5 Prescalar design using three D-Flip-flop, a NOR and NAND gate.

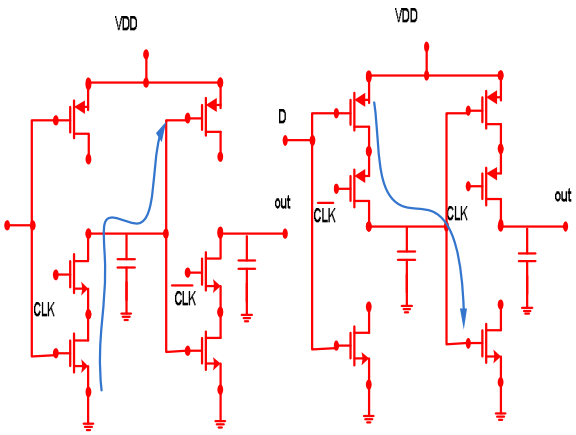

Fig. 8. Precharge and evaluation phase C^2MOS logic D-Flip flop.

VII. DIVIDE-BY-4/5 COUNTER USING DOMINO LOGIC

Extended True Single Phase Clock form of divide-by-4/5 counter is designed with domino logic for high speed and reduce noise immunity in the circuit. The Extended True Single Phase Clock is used to increase the higher operating frequency by reducing the number of transistors used. The circuit diagram which shows the working principles is given below From the Fig 8, the E-TSPC form of D Flip-Flops (DFF) are connected together. The divide-by-4/5 counter consists of three flip-flops and one negated AND (NAND) gate and negated OR (NOR) gate. The NAND gate connected in front of the DFF1 and domino logic is connected between the both DFF1 and DFF2. Then the NOR gate is connected before the DFF3. The MOS transistors are act as switches.

The Metal Oxide Semiconductor (MOS) is turned on or off depending on the gate voltage. In Complementary Metal Oxide Semiconductor (CMOS) technology, both n-channel (and nMOS) and p channel MOS (or pMOS) devices exist. The nchannel MOS device requires a logic value 1 (or a supply Vdd) to be "on" the p-channel MOS device requires a logic value 0 to be "on". The MC signal is used to control the circuit.

VIII. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

Simulation of 4/5 prescalar is done on Cadence using specter simulator. Conventional NAND and NOR gate were used for the designing of the 4/5 prscalar for maintaining the proper voltage level of operation. And ETSPC D-flip flop is used for high speed operation. The schematic of D-flip flop ,NAND, NOR is shown in fig 9.,fig 10.,and fig 11. and overall block diagram is shown in figure 12.

Simulation result of D-flip flop, NAND, NOR and overall schematic is shown in figure 13, figure 14, figure 15 and figure 16.

And power distribution of the D-flip flop, NAND, NOR and overall schematic is shown in figure 17, figure 18, figure 19 and figure 20. And jitter response diagram is shown in figure 21.

Comparison table with previous work is shown in table I

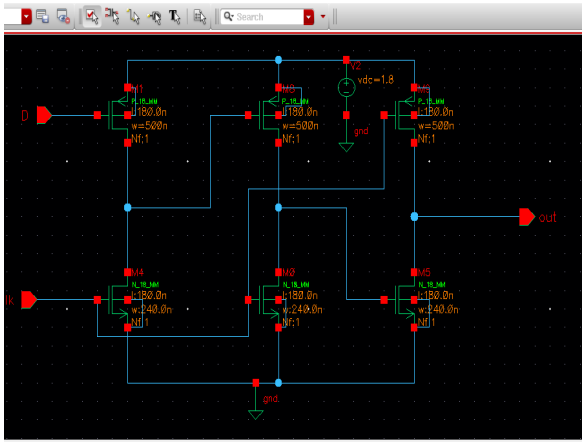

Fig. 9. Schematic of ETSPC D-Flip flop.

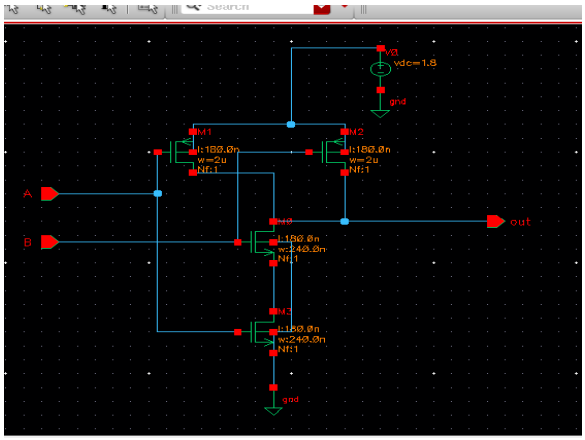

Fig. 10. Schematic of NAND gate.

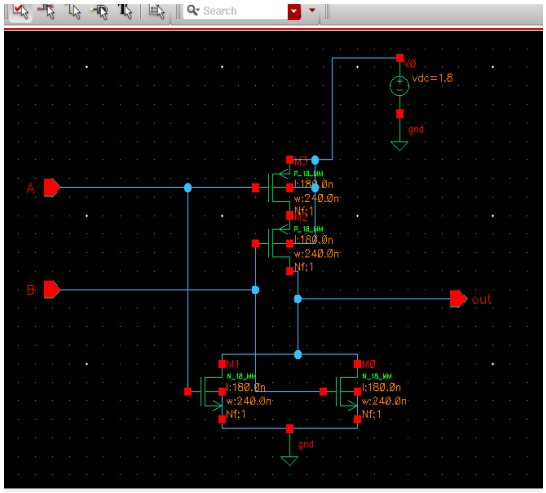

Fig. 11. Schematic of NOR gate.

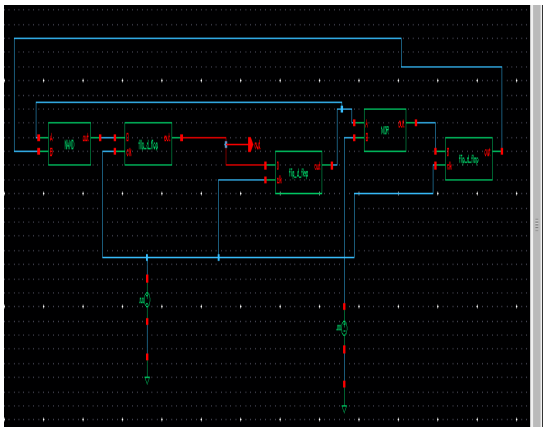

Fig. 12. Block diagram of 4/5 prescalar.

	Ref [17]	Ref [18]	Ref [1]	Proposed
Design	2/3 counter	2/3 counter	2/3 counter	4/3 counter
Transistor count	16	16	13	26
Max freq(Mhz)	475	470	531	1000
Average Power(uW)	6.4	5.75	4.6	50
Power delay product(fJ)	13.43	12.2	8.2	45
Jitter(ps)	13.7	10.01	7.02	1.2
Technology CMOS			180nm	180nm

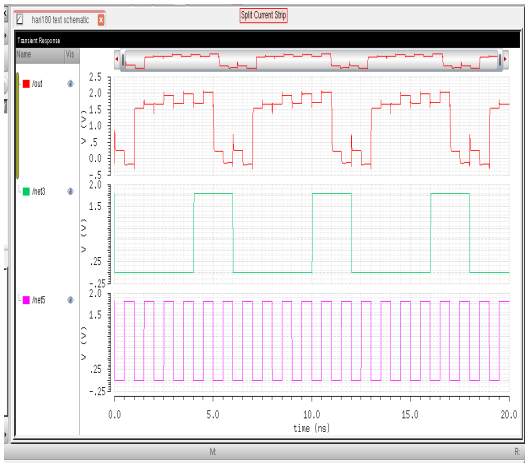

Fig. 13. Simulation of ETSPC D-Flip.

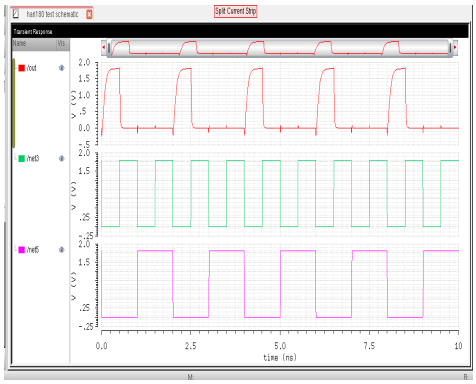

Fig. 14. Simulation of NOR gate.

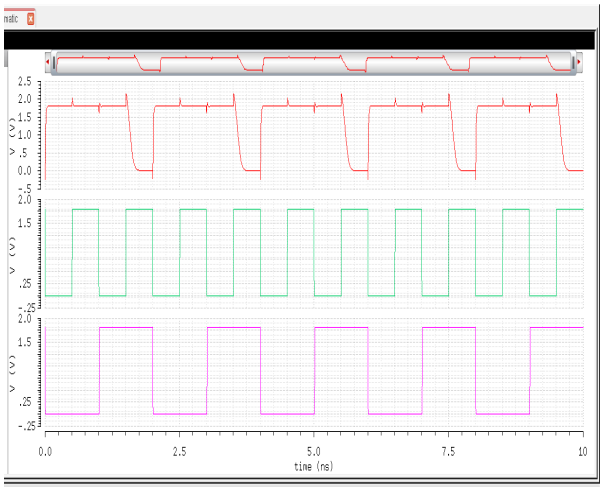

Fig. 15. Simulation of NAND gate.

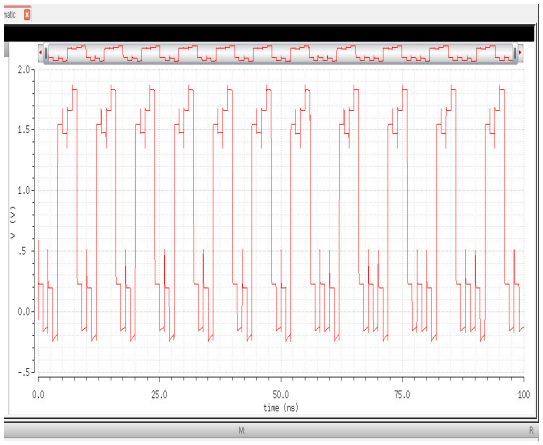

Fig. 16. Simulation of ETSPC 4/5 prescalar.

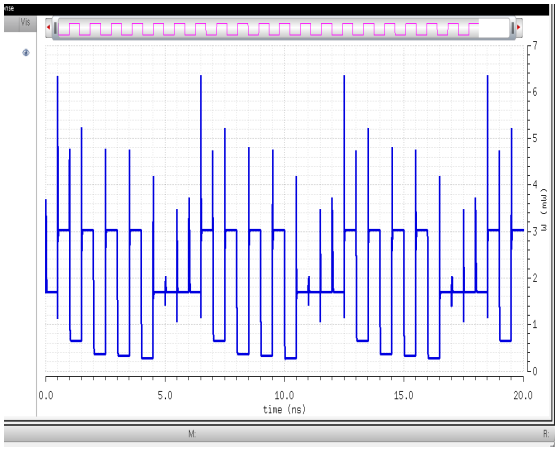

Fig. 17. Power consumption of ETSPC D-Flip.

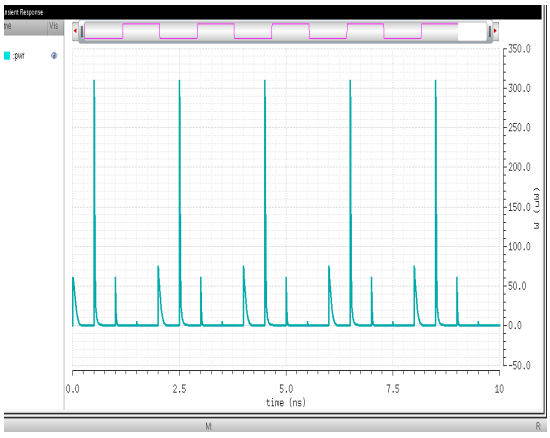

Fig. 18. Power consumption of NOR gate.

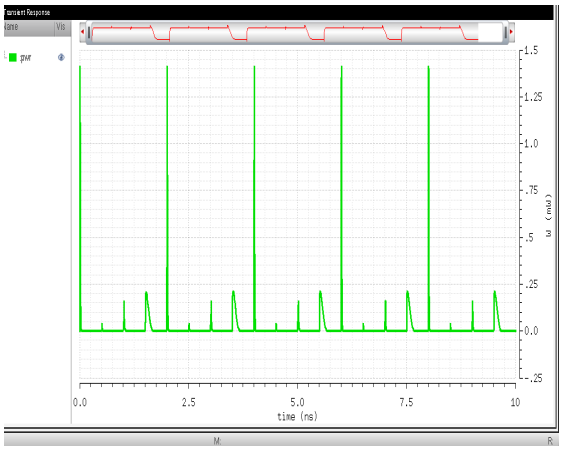

Fig. 19. Power consumption of NAND gate.

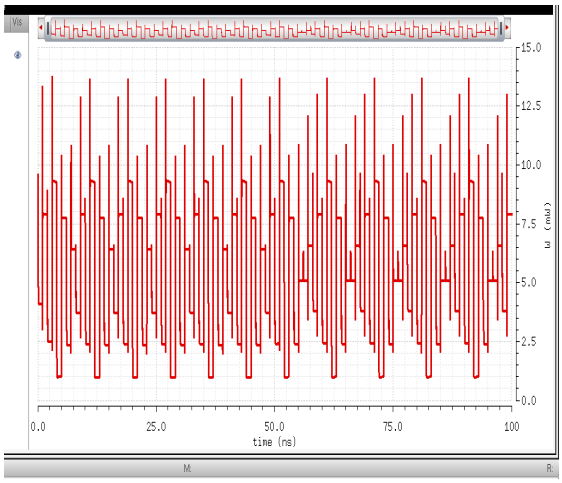

Fig. 20. Power consumption of 4/5 Prescalar.

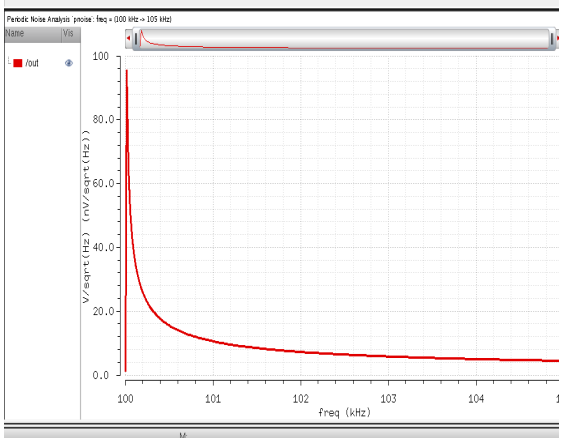

Fig. 21. Jitter response of 4/5 prescalar.

CONCLUSION

The proposed 4/5 prescalar work fine under 180 nm CMOS UMC technology with 1.8 volt supply. Conventional CMOS NAND & NOR is used for proper voltage regulation in between circuit. With jitter of 1.2 ps.

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